

Electronic Acknowledgement Receipt

EFS ID:	2989013
Application Number:	10659974
International Application Number:	
Confirmation Number:	5045
Title of Invention:	CHANNEL BONDING OF A PLURALITY OF MULTI-GIGABIT TRANSCEIVERS
First Named Inventor/Applicant Name:	Joseph Neil Kryzak
Customer Number:	24309
Filer:	Justin Liu/Katherine Stofer
Filer Authorized By:	Justin Liu
Attorney Docket Number:	X-1367 US
Receipt Date:	12-MAR-2008
Filing Date:	11-SEP-2003
Time Stamp:	20:14:44
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$810
RAM confirmation Number	4119
Deposit Account	240040
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)

1	Foreign Reference	EP_0315275_A2.pdf	818323 73b17b0444bbcb3e9fc21c10fb41b1 a525503d	no	12
Warnings:					

Information:

2	Foreign Reference	WO_9325968A1.pdf	1145636 5c1d69d8163483be4dd5ce14482e80 b4ce90db	no	30
Warnings:					

Information:

3	Foreign Reference	EP_0905906A2.pdf	502067 657535d0778bc6b4b24e27f3aa3-bbbe 7c2de1fa5	no	10
Warnings:					

Information:

4	Foreign Reference	EP_1235351A1.pdf	505729 04b5251e02b69729e304b97a4add127 06150884	no	11
Warnings:					

Information:

5	NPL Documents	Albaharna_Area_and_Time_NPL.pdf	501011 9f19915bd2ce54b1f64a114c891b0511 cf05a4	no	6
Warnings:					

Information:

6	NPL Documents	Andrew_A_Field_Prog_NPL.pdf	386491 6396605495071ddcbe5ed5b7140c6512 f5d5057e	no	5
Warnings:					

Information:

7	NPL Documents	Carter_The_Future_of_Programmable_NPL.pdf	586523 216d3c6998cc8489d1a5b3951fb79b 76ebx35d	no	8
Warnings:					

Information:

8	NPL Documents	Davidson_FPGAImplementation_NPL.pdf	232306 624ab3d0f7e9fb9a2bdc39a54108695 72hec79	no	4
Warnings:					

Information:

9	NPL Documents	DeHon_DPGA_Coupled_NP_L.pdf	798451 898ebc93265ec94b334e834e21bbcd27 4320e374	no	10
Warnings:					

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10	NPL Documents	French_A_Self_reconfiguring_NPL.pdf	813885 bf6e1be4dc79ed9424d5120c20a4ebfa d7fb2225	no	11
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Information:

11	NPL Documents	IBM_32Bit_NPL.pdf	6761375 793b29addb4a151b8e4ebcd1dd0d5 e9fb10fc	no	140
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Warnings:
Information:

12	NPL Documents	IBM_Powerpc_405_NPL.pdf	18215204 ed60956c903898c3d0f5b5127cb91b99 12x0211	no	550
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Warnings:
Information:

13	NPL Documents	Iseli_A_C_Plus_Plus_Compiler_NPL.pdf	446551 9fa4c113130234b65a1a1fb79b52b3dc 71a4792	no	8
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Warnings:
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14	NPL Documents	Iseli_Beyond_Superscaler_NPL.pdf	255066 d23864c63b2c3f162a452701b3b3a54 98285e5d	no	5
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15	NPL Documents	Iseli_Spyder_A_Reconfigurable_NPL.pdf	442425 2994ae17276c4fe52b5a9cabe79367 9b9ee75	no	8
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16	NPL Documents	KiaeI_VLSI_Design_of_Dynamically_NPL.pdf	270396 ba6e993ec1566db8a1a12952fa1a59c 83ce366	no	5
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17	NPL Documents	Maki_A_Reconfigurable_Data_NPL.pdf	256368 abae705c19954119a1b80c1b6551bb4 b10d2ns40	no	4
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18	NPL Documents	Snyder_Xilinx_A_to_Z_NPL.pdf	490110 93013170d8b383e141187945eb0f7395 667b9963	no	5
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19	NPL Documents	Snini_Field_Programmable_Gate_NPL.pdf	495908 8633b3a7e243b52d983442bc18195 4e41be8	no	6
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Warnings:**Information:**

20	NPL Documents	Wirthlin_The_Nano_Process_or_NPL.pdf	711475 e07063b6edfb4a0a4362e2501bd36 cefb6cb	no	10
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Warnings:**Information:**

21	NPL Documents	Wittig_OneChip_an_FPGA_NPL.pdf	1023485 55e830f0cced8a295cab4d520ba5a1d 3e0009e	no	11
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Warnings:**Information:**

22	NPL Documents	Xilinx_Programmable_LDB_1994_2_9_to_2_18_NPL.pdf	1066027 6417954074350a1e601abed12d9915 e9e953452	no	13
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Warnings:**Information:**

23	NPL Documents	Xilinx_Programmable_LDB_1994_2_107_to_2_108_NPL.pdf	331834 629220e381350b73a45719ee5896aa1 393967c	no	5
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Warnings:**Information:**

24	NPL Documents	Xilinx_Programmable_LDB_1994_2_109_to_2_117_NPL.pdf	773523 299459636bd227014c3c675ebc1764 e50a29b28	no	12
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Warnings:**Information:**

25	NPL Documents	Xilinx_Programmable_LDB_1994_2_187_to_2_199_NPL.pdf	1156817 037a157122468e00c0ab8d25a97124 e1f9971	no	16
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Warnings:**Information:**

26	NPL Documents	Xilinx_Programmable_LDB_1999_3_1_to_3_50_NPL.pdf	3031136 8001432ff352e3d894e804d59795bbe 3721421	no	54
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Warnings:**Information:**

27	NPL Documents	Xilinx_Programmable_LDB_2000_3_1_to_3_117_NPL.pdf	7056683 664bd6fb7e119b956f0204e07524ba5 a26471d	no	122
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Warnings:**Information:**

28	NPL Documents	Xilinx_Programmable_LDB_2000_3_7_to_3_87_NPL.pdf	2219494 494786481bd3ed351f7299667b55021 651ea903	no	27
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29	NPL Documents	Xilinx_Virtex_Two_Platform_FPGA_Hndbk_NPL.pdf	3105531 246966095af30e271362819832fbefb5 86142b0	no	45
Warnings:					
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30	NPL Documents	Yamin_Aizup_A_Pipelined_NPL.pdf	501670 059d38abdaa59864ca1e112a144d35 8c972a11	no	9
Warnings:					
Information:					
31	NPL Documents	Xilinx_Programmable_LDB_1994_rv_1995_Part1_pgs_1_to_345_NPL.pdf	21297550 e873fe5733521cc09986c2f3f53803fbfa 43c0cc5	no	345
Warnings:					
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32	NPL Documents	Xilinx_Programmable_LDB_1994_rv_1995_Part2_pgs_3_46_to_689_NPL.pdf	20651519 c50d59b055770d5aa8963546d23469 bf20fb64c7	no	344
Warnings:					
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33	Request for Continued Examination (RCE)	X1367_US_RCE_WIDS_efile_d.pdf	627252 2251ce1587cd29510ec2c2bfff99b6d4641 e0ne91	no	3
Warnings:					
Information:					
34	Information Disclosure Statement (IDS) Filed	X1367_US_SB08A_efiled.pdf	130890 5a374aac92d990f528c1468f84e495240 d3330dd2	no	7
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
35	Fee Worksheet (PTO-06)	fee-info.pdf	8205 e0047b50633495e-08a295414a32806 d412924c	no	2
Warnings:					
Information:					
Total Files Size (in bytes): 97616916					

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.